Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **+ ERROR**
2. **– ERROR**
3. **COMP**
4. **CSS**
5. **N. RESET**
6. **– CURRENT SENSE**
7. **+ CURRENT SENSE**
8. **N. SHUTDOWN**
9. **RTIMING**
10. **CT**
11. **RD**
12. **N. SYNC**
13. **OUTPUT A**
14. **VCC**
15. **GROUND (2pads)**
16. **OUTPUT B**
17. **+ VIN**
18. **VREF**

**.097”**

**15**

**13**

**3 2 1 18 17 16**

**8 9 10 11 12**

**4**

**5**

**6**

**7**

**14**

**.116”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: GND**

**Mask Ref: HJ**

**APPROVED BY: DK DIE SIZE .097” X .116” DATE: 4/27/23**

**MFG: UNITRODE THICKNESS .015” P/N: UC1526**

**DG 10.1.2**

#### Rev B, 7/19/02